Integration of a Photonic Clock Rate Multiplier with Global Distribution in Microprocessors

James P. Siepmann
Chief Research Officer, LightTime, 375 City Center, Oshkosh, WI 54901
Email: Siepmann@LightTime.com Web: www.LightTime.com

Abstract: Presented is a novel on-chip optical rate multiplier that can increase a microprocessor's photonic clock signal up to twenty-fold and serve as the global interconnects for regional signal distribution. This design allows for the use of low-cost components while still achieving clock rates in excess of 40 GHz.

I. INTRODUCTION

One of the major hurdles to the implementation of photonic clocking is the finding of a scalable and cost-effective photonic clock generation solution and a distribution mechanism. We present here a novel optical rate multiplier that can increase a photonic clock signal up to 20-fold as well as serving as the mechanism for global photonic signal distribution in a microprocessor.

Photonic clocking of microprocessors is inevitable; the only question is when it will occur. Problems with keeping the current copper based electrical interconnect are anticipated to begin in 2007[1] and Intel anticipates its switch from electrical to optical to occur during a 2008-2012 high-volume manufacturing (HVM) cycle.[2] Switching from electrical to optical will entail the implementation of on-chip optical waveguide interconnects and an optical clock to provide the signal source. With ITRS anticipating on-chip clock rates being in excess of 10 GHz by 2008 and over 20 GHz by 2012, a scalable photonic clocking system will be needed.[1]

Though economical passively modelocked semiconductor lasers are available that can be implemented for a 2008-2012 HVM cycle, this paper presents another low-cost alternative. By using a closed loop optical pulse multiplier (OPM) that can also distribute the multiplied clock signal to different cores and regions, an optical clock signal can be increased over 20-fold.

Optical pulse multipliers for clocking is not a new idea, with its origin and patenting dating back to the last decade but using an embodiment of these earlier devices[3] as a distribution mechanism is. Additionally, we present the necessary design formulas and demonstrate the optical pulse multiplication of a 2 GHz signal to 40 GHz.

II. EXPERIMENT

For this experiment we could have used both direct or indirect modulation of a CW laser with no significant difference in the results as long as the optical signal into the OPM was comparable. In this instance, a 1550 nm laser was used to generate a 2 GHz photonic clock with a pulse width of 40 ps FWHM. In order to demonstrate different frequency outputs from a single device, optical fiber was used as a waveguide with a variable delay. Though a single tap with a photodetector (PD) was used to represent the on-chip signal distribution, this could have been multiple taps whose combined waveguide and tap losses was 40%. A 50GHz PD was used for opto-electrical conversion and an oscilloscope with a bandwidth of 50 GHz was used for the measurements.

The length of the OPM loop (or a harmonic thereof) for a given f_i can be determined by the following formula:

$$d = (1 \pm 1/M)\, c \,/\, (\eta\, f_i)$$

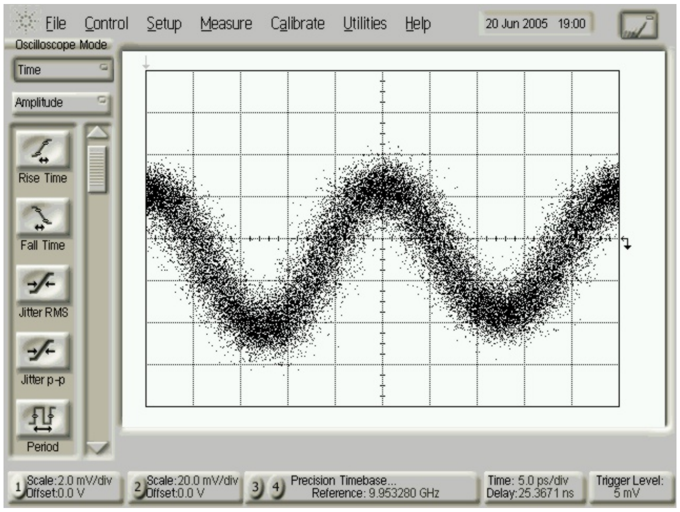
where d is the loop length, M is the multiplication factor, c is the speed of light in a vacuum, and η is the refractive index of the waveguide being used. The loop lengths used (or harmonics thereof) are shown in Table 1 as well as several examples of using a fixed loop length while varying f_i. The loop lengths for a waveguide with a η=3 were also shown for comparison.

f_i GHz	M	d (η=1.47) cm	d (η=3.00) cm	f_o GHz
2	3	6.80	3.33	6
2	4	7.65	3.75	8
2	5	8.16	4.00	10
2	9	9.07	4.44	18
2	14	9.48	4.64	28
2	16	9.57	4.69	32
2	19	9.67	4.74	38
2	20	9.69	4.75	40
1.5	4	10.20	5.00	6
1.75	8	10.20	5.00	14
1.875	16	10.20	5.00	30

Table 1. OPM data for various loop lengths and optical input frequencies.

III. RESULTS

When using a f_i of 2 GHz, we were able to achieve pulse multiplication up to 20-fold (M=20), which in this case was 40 GHz as shown in Fig. 2.



1 Scale:2.0 mV/div Offset:0.0 V
2 Scale:20.0 mV/div Offset:0.0 V
3 4 Precision Timebase... Reference: 9.953280 GHz
Time: 5.0 ps/div Delay:25.3671 ns
Trigger Level: 5 mV

Fig. 2. Oscilloscope picture of the experimental OPM using a f_i of 2 GHz and yielding a f_o of 40 GHz (5 ps/div).

IV. DISCUSSION

For a microprocessor with an edge length of 1 cm or greater it is easy to see how a waveguide could be created at the outer edge with internal branching as shown in Fig. 4. Furthermore, H-tree waveguides (with appropriate curvature for acceptable losses) could be used to further decrease power, heat, EMI, crosstalk, jitter, skew, and more as well improving signal integrity.[4]

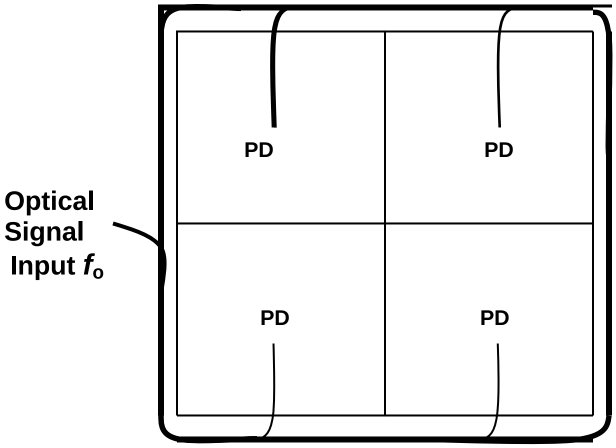


Fig. 4. Potential microprocessor OPM design for optical signal multiplication and distribution.

In order to provide equal optical power to each PD, each tap will need to be designed with a different ratio. For instance, if a 60% total tap loss is desired for each loop cycle, then a four tap design would need to use sequentially outputs of 20%, 25%, 33%, and 50% respectively. The formula for calculating each tap ratio is:

$$\text{tap}_N = P/(100\% - P(N-1))$$

where N is the sequential number of the tap (e.g. 1, 2, 3, etc.), and P is the desired percentage of the loop's initial power that is desired for each individual tap.

Different materials could be used such as SiON, Si_3N_4, SiO_2, Si, or a polymer, to create waveguides in a silicon microprocessor. Because of economic pressures, those waveguides which can be created with current CMOS technology or a low-cost alternative are likely to prevail.

One of the prototype modulator/drivers that we have used in an OPM is relatively simple and low-cost, and yet it is able to produce pulse widths less than 75ps and can be triggered by most off-the-shelf voltage controlled oscillators running in the sub-GHz to multi-GHz range. We have also used optical feedback which has intriguing implications in this situation.

With the advent of multi-core processors and longer distances that a clock signal will need to travel, a photonic clock solution may be a viable alternative, especially when it also serves as the distribution mechanism.

REFERENCES

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